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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,162	12/06/2001	Charles E. Nichols	01-758	2861

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LSI Logic Corporation
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EXAMINER	
GOSSAGE, GLENN A	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,162	NICHOLS ET AL.	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 5, lines 9 and 11, it appears "example" should be --exemplary-- for clarity. See also page 8, line 7 and page 9, line 12. In line 15, it appears "5, a" should be --5 is a--, and "is shown" deleted for clarity and consistency (see lines 13-14, e.g.).

On page 6, line 4, it appears "limited" (first occurrence) should be changed to --intended-- for clarity. In line 7, the wording "principles of the invention the practical application to enable" is not clear. In lines 16 and 17, and throughout the specification, all trademarks and trade names, and their respective owners, should be properly identified, if appropriate. See MPEP 608.01(v). In line 22, it appears "A" should be --An--.

On page 10, line 9, it appears --the process-- should be inserted before "allocates" for clarity (for parallel sentence construction, e.g. Note page 11, line 1.).

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 15, line 2, it appears --the-- should be inserted before "write" (first occurrence) for consistency (see claim 11, line 8).

In claim 18, line 4, it appears "memory controller" should be --first controller-- for clarity (to provide a proper antecedent for "the first controller" in claims 19 and 22, line 4, e.g.). Also, it appears "that manages a connection to a memory" should be deleted for clarity (the connection or relationship between the memory in claim 18, line 4 and the first (second) memory or memory pool in claims 19, 22-23 and 25 is not clear).

Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Chong, Jr.

With respect to claims 1 and 7, Chong, Jr. discloses a method for managing a read request including receiving, at a first controller, a read request for a data block [see controller 26 in Figure 4A, as well as corresponding parts of Fig. 5, and column 4, lines 68-71], and allocating a memory buffer for the data block from a memory pool that includes a first memory on the first controller and a second memory on a second controller, wherein the memory buffer resides in the second memory [Chong, Jr. teaches that a cache memory may be allocated to buffer data, where the buffer may be allocated from a memory pool including a first cache memory 341 and a second cache memory 342. Chong, Jr. also teaches that space may be allocated in the first cache memory and in the second cache memory to mirror the data and provide improved reliability (see column 7, lines 11-13; column 8, line 63 to column 9, line 1; column 11, lines 64-66; and column 12, lines 6-9 and 17-21, e.g.).].

Also with respect to claim 1, Chong, Jr. further teaches retrieving the data block from a storage device [16 in Fig. 4A and 161, 162 in Figure 5] and caching the data block in the memory buffer [see column 7, lines 11-13, e.g.].

With respect to claim 11, Chong, Jr. also discloses that the system may be used to manage write requests in addition to read requests wherein a write request for a data block is received at the first controller (see column 4, lines 58-59, e.g.). Chong, Jr. discloses that a "primary" data buffer for the data block may be allocated in a first cache memory and a mirror data buffer allocated for mirroring the data block in a second memory, wherein the first memory resides on one of the first controller and a second controller and the second memory resides on the other of

the first controller and the second controller [see column 7, lines 6-11 and column 11, lines 64-6]. Write data for a data block may be stored in the "primary" data buffer and mirrored in the secondary or mirror data buffer as discussed above.

With respect to claims 2, 8 and 12, Chong, Jr. discloses that the first controller includes a first switch (221 in Fig. 5) and the second controller includes a second switch (222 in Fig. 5).

With respect to claims 3, 9 and 13, Chong, Jr. discloses that the first switch and the second switch are coupled using a switch-to-switch path [note the bus or path between the switches in Fig. 5, for example].

With respect to claims 4 and 10, a data block may be cached or mirrored in the second memory via the switch-to-switch path [see column 8, line 63 to column 9, line 1 and column 11, lines 64-66, e.g.].

With respect to claims 5 and 16, a data block may be retrieved from or written to a storage device in Chong, Jr. using a drive adapter on the second controller via the switch-to-switch path [Chong, Jr. teaches that a data block may be retrieved from either storage device to provide improved reliability. Note that the storage devices includes some kind of "adapter" or controller (not shown) for connection to the bus or switch (see column 5, lines 46-49, as well as column 9, lines 8-10, e.g.)].

With respect to claims 6 and 17, Chong, Jr. discloses that a data block may be retrieved from or written to a storage device using a drive adapter on the first controller via the first switch [see

Fig. 3A, e.g., and again note that the storage device includes some kind of "adapter" or controller].

With respect to claims 14 and 15, either cache memory or buffer may be considered to be the "first" memory serving as the "primary" data buffer with the other "second" cache memory or buffer serving as the mirror data buffer.

With respect to claim 18, Chong, Jr. discloses an "apparatus" in a first controller [26 in Fig. 4A, e.g., as well as corresponding parts of Fig. 5] including a host adapter that provides a connection to a host [see hosts 121 and 122 in Fig. 5 and also see column 9, lines 8-10], a processor [see CPUs 241, 242 in Fig. 3A and column 5, lines 5-7, e.g.], a memory controller that manages a connection to a memory [see column 7 lines 37-39], a drive adapter that provides a connection to a storage device [the storage devices 16 and 161, 162 include some kind of "adapter" or controller (not shown) for connection to the bus or switch (see column 5, lines 46-49, as well as column 9, lines 8-10, e.g.)], a first switch that connects the host adapter, the processor, the memory controller, and the drive adapter [see switch 221 in Figure 5, e.g.] and a switch-to-switch path that connects the first switch to a second switch on a second controller [see second switch (222 in Fig. 5) coupled to the first switch by a "switch-to-switch path" (note the bus or path between the switches in Fig. 5, for example)].

With respect to claim 19, as well as claim 22, Chong, Jr. also discloses managing a read request including receiving, at a first controller, a read request for a data block, allocating a memory buffer for the data block from a memory pool that includes a first memory on the first

controller and a second memory on a second controller, wherein the memory buffer resides in the second memory, retrieving the data block from a storage device and caching the data block in the memory buffer [see the discussion above with rspect to claim 1].

With respect to claims 20-21 and 23-27, attention is respectfully directed to the discussion above with respect to claims 6, 5, 11, 14, 15, 17 and 16, respectively, which use similar language.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yanai et al is cited as disclosing a data storage system having first and second controllers including first and second cache memories, a plurality of disk adapters and a plurality of channel adapters similar to the present invention.

DeKoning et al is cited as disclosing a method and apparatus for managing read and write requests in a data storage system having first and second controller, each including a processor and a local memory similar to the present invention.

Ofek is cited as disclosing a method and apparatus for providing independent access to data in a data storage system having first and second buffer memories storing mirrored data.

Hubis is cited of interest as disclosing a storage system including first and second controllers and first and second cache memories storing mirrored data similar to the claimed invention.

Hodges is cited as disclosing a storage system having first and second controllers and utilizing locking to provide data synchronization or coherency.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187